SELF-ALIGNED PHASE SEPARATION FOR IBC CELLS USING PVD POLYSILICON

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ABSTRACT: We introduce an innovative IBC solar cell process leveraging the directional deposition nature of doped polycrystalline silicon (poly-Si) through physical vapor deposition (PVD). This method enables the self-alignment of passivated contacts, effectively separating the polarities. The self-aligned back contact (SABC) cell incorporates n-type and p-type passivated contacts, achieved through interfacial oxide (SiO_X) and doped n- and p-type poly-Si layers respectively, arranged in an interdigitated design on the back side. The insulation between the p-type and n-type poly-Si layers requires only a single structuring process of the firstly deposited p-type poly-Si. The subsequent blanket deposition of n-type poly-Si by PVD remains insulated from the p-type poly-Si layer due to the self-alignment properties inherent in our structuring and deposition processes. The SABC target process sequence can be implemented into existing TOPCon manufacturing lines requiring only two additional processing tools.
Keywords: IBC, TOPCon, passivating contacts, self-alignment

1 INTRODUCTION

The SABC solar cell[1] implements an interdigitated back contact (IBC) design, featuring passivating poly-Si on silicon oxide (poly-Si/SiO_X) contacts of both polarities on the rear side on n-type silicon wafers. The passivating contacts of opposite polarity are not insulated by a dedicated trench, but by an undercut in the trench wall itself. The trench is needed anyway to pattern the first poly-Si and create space for the second poly-Si to form the contact to the base. When etching the trench into the p-type poly-Si, the poly-Si layer is intentionally under-etched. We then utilize the directional nature of PVD of the second poly-Si to prevent its deposition underneath the under-etched first poly-Si layer, thereby achieving an insulation of the opposite doped poly-Si layers without the need for additional structuring or masking. The n-type poly-Si, located at the bottom of the trench, has already demonstrated its excellent passivating properties yielding $iV_{OC} > 735$ mV [1,2].

The proposed process flow for manufacturing the SABC solar cell builds upon the standard TOPCon process. The transition from TOPCon to SABC requires minimal adjustments, involving only four additional processing steps, two of which require new tools: laser structuring of the first poly-Si layer and for the PVD deposition of the second poly-Si layer. The other two steps can be implemented on existing tools of the TOPCon process: PECVD deposition of an etch mask and wet chemical cleaning. Beyond these additions, the SABC process also requires the deposition of in-situ doped p-type poly-Si in a LPCVD tool formerly used for n-type or intrinsic poly-Si deposition.

In this contribution we present the SABC cell concept and evaluate a possible process sequence. Furthermore, our optimized p-type poly-Si/SiOx layer stack deposited by LPCVD demonstrates an excellent $J_0 = 2.3$ fA/cm², similar to previously reported values [3], and we show SEM images of the under-etched trench. We also provide proof of concept with a first solar cell yielding an efficiency of $\eta = 20.2\%$.

[1] Patent pending.

2 EXPERIMENTAL

2.1 SABC solar cell concept and process flow

Figure 1 a) illustrates the SABC solar cell design and figure 1 b) outlines a possible processing sequence. Unlike other IBC concepts with two TOPCon passivating contacts, often referred to as TBC [5], this approach requires no dedicated trench to insulate the poly-Si layers of opposite polarity. Instead, the undercut of the trench wall separates the two polarities, where the first p-type poly Si layer (emitter) lies atop the trench surface, while the second n-type poly-Si is located at the bottom of the

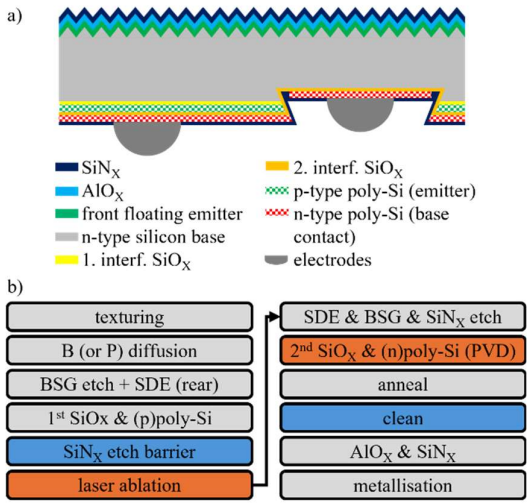


Figure 1: a) Sketch and b) process sequence of a self-aligned back contact (SABC) cell. The IBC cell with passivating poly-Si/SiO_X contacts features an insulation of the poly-Si layers of opposite polarity by separating the layers only across the undercut along a trench wall. Compared to a conventional TOPCon process, this process only requires two additional processing tools (orange) and another two fabrications steps (blue) which can be implemented on existing tools.

trench. Underneath the undercut, which realised by wet chemical etching of the trench, no poly-Si is deposited during the PVD process. The n-type poly-Si also covers the p-type poly-Si emitter forming a low resistive tunnelling contact, as both poly-Si layers are highly doped with dopant concentrations exceeding $C = 10^{20}$ cm^{-3}. The n-type poly-Si layer covers the full surface and enables the use of the same metallization scheme for both polarities.

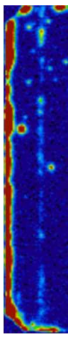
Figure 1b) illustrates one possible process sequence and highlights the additionally required fabrication steps to a standard TOPCon process in orange and blue. The orange highlighted steps require two additional tools, while for the blue coloured steps an existing PECVD tool and wet bench can be used respectively. Furthermore, the n-poly-Si in a TOPCon process is deposited either in-situ doped or intrinsic in the LPCVD tool. This tool requires retrofitting to deposit p-type silicon, while the $POCl_3$ diffusion furnace (in the case of ex-situ doped n-poly) is used for SABC's annealing step. Other slightly modified sequences may be advantageous, depending on the TOPCon process of the base line.

In accordance with TOPCon, the SABC target process starts with texturing and boron diffusion on both front and rear. A single side BSG etch followed by alkaline etching of the boron emitter on the rear prepares this surface for the poly silicon deposition. Instead of the boron diffusion forming the front floating emitter (FFE), a phosphorus diffusion forming a front surface field (FSF) or an un-diffused surface could be used for the SABC process flow as well. Advantageously, a phosphorus-diffused surface typically yields better surface passivation than a boron-diffused surface [6]. After depositing interfacial oxide and p-type poly-Si by LPCVD on both the front and rear side, the rear side receives a PECVD-deposited SiNx etch barrier. Laser ablation locally removes the SiNx layer and exposes the poly-Si in the typical IBC pattern. Alkaline wet chemical etching strips the poly-Si on the front side up to the BSG layer and on the rear etches the p-type poly-Si in the exposed areas. The etching on the rear not only removes the poly-Si layer, but also etches the silicon base vertically and lateral, creating an undercut of the surface. Even after removal of the barrier layer, the poly-Si and trench edge will shadow a significant part of the trench wall. After etch barrier (rear) and BSG (front) removal and growing a second interfacial oxide, the subsequently deposited n-type poly-Si by PVD will not cover the full surface on the rear. With the highly directional deposition technique, the doped silicon mainly deposits on vertically exposed surfaces, i.e. surfaces not being shadowed by the undercut. Hence, at the bottom of the trench n-type poly-Si forms a passivating contact but there will also be an n-type poly-Si on top of the p-type poly-Si forming a tunnel junction to the emitter. The shadowed part of the trench wall insulates both passivating contacts, without the need for additional processing steps like structuring, local etching or masking. The SABC process finishes with high temperature annealing, crystallising the poly-Si layers and activating the dopants, standard passivation with AlO_x and SiN_x and metallisation by screen printing. Since the n-type poly-Si covers the surfaces of both passivating contacts, the same screen-printing paste may be applied in a single printing step for both polarities.

The passivation quality of the p-type poly-Si/SiO_X layer was investigated and optimized at ISFH on symmetrically processed n-type wafers, passivated with a PECVD SiN_X layer and fast firing. Three different interfacial oxides were annealed at different temperatures to find the optimum process window in terms of sheet resistance and surface passivation.

Scanning electron microscopy (SEM) images inspect the n-type poly-Si deposited at the trench cross section and show separation of the layer at the under-cut. The sample preparation includes laser ablation of an etch barrier on top of a p-type poly-Si, wet chemical etching of the poly-Si and up to 10 µm of the bulk, and subsequent etching the barrier layer. Then, to enhance the contrast between n-poly silicon and bulk wafer, an 80 nm dielectric layer by PECVD is deposited followed by the PVD n-type poly-Si layer. Laser scribing enables cleaving in a 90 ° angle to the trench direction.

For the SABC cell processing at ISFH, we are currently using a slightly different process flow than depicted in figure 1b): Utilizing BSG as an etch mask for alkaline etching requires additives that are not yet available in the standard wet bench. Hence, the cells feature a non-diffused front surface and single side acidic polish on the rear to remove the texture. Additionally, we apply ISFH's standard p-type poly-Si LPCVD deposition process yielding the excellent results in figure 2, which includes a dedicated annealing of the p-type poly-Si layer. Presently, in the SABC cell processing the p-poly layer receives a second anneal required for n-type poly-Si crystallisation, leading to an iV_{OC} drop below the target value, as too much boron diffuses into the silicon bulk, increasing J_{0e} of the emitter, which is subject to future improvements.



3 RESULTS AND DISCUSSION

3.1 p-type poly-Si surface passivation

Figure 2 a) shows sheet resistance R_{sh} and figure 2 b) J_{0e} of a 200 nm thin p-type poly-Si emitter deposited by LPCVD on three different oxides and annealed in an inert atmosphere at temperatures between 820 °C and 900 °C. All oxides achieved their lowest R_{sh} at the maximum investigated annealing temperature T = 900 °C. However, the J_0 yields its lowest value $J_0 = 2.3$ fA/cm² at 880 °C with a median of $J_0 = 5.1$ fA/cm². This corresponds to maximum $iV_{OC} = 739$ mV and, in combination with the low $R_{sh} \approx 154$ Ω/sq, promises a high efficiency potential when applied to a SABC solar cell. The same test run included wafers annealed with an oxygen atmosphere at T = 860 °C (not shown). The resulting oxide layer can serve as an etch barrier for the subsequent wet chemical etching of the poly-Si. For this particular group the median $J_0 = 6.7$ fA/cm² stands only marginally higher than the samples subjected to the inert annealing. The sheet resistance $R_{sh} \approx 303$ Ω/sq is notably higher, as the surface of the poly-Si oxidizes and consumes a substantial amount of the boron dopants. This oxidized p-type poly-Si still forms the emitter of the solar cell described below, but the oxidation is targeted to be skipped in the future, as we expect too much in-diffusion of boron into the bulk, if a second annealing step is applied for crystallization of the n-type poly-Si.

3.2 N-type poly-Si insulation

Figure 3 shows a SEM image of the cross section of one side of an anisotropic etched trench with a dielectric and n-type poly-Si layer. The p-type poly-Si is etched slower than the lowly doped n-type c-Si wafer resulting in approximately 0.5 µm poly-Si overhang on the wafer surface. Additionally, the anisotropic etch removes the Si

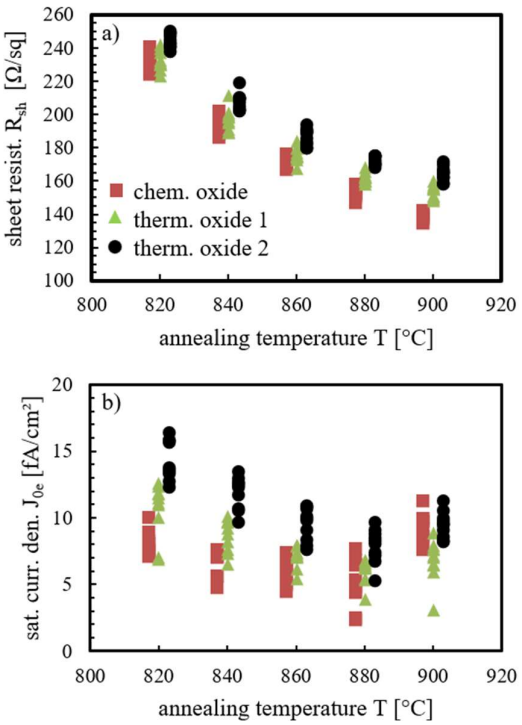


Figure 2: a) Sheet resistance R_{sh} and b) saturation current density J_{0e} for p-type poly-Si deposited by LPCVD at ISFH. All oxides were annealed at the same temperature and are only displayed next to each other for better visualisation. Annealing at T = 880°C yields the lowest J_{0e} = 2.3 fA/cm² and sufficiently low R_{sh} = 154 Ω/sq.

faster into the <111> direction resulting in an additional undercut with a 54° angle. The SiN_X layer, deposited be PECVD to enhance the contrast between n-type poly-Si and c-Si wafer, wraps itself around all exposed surfaces, but does appear to be thinner underneath the trench. The n-type poly-Si however is mostly deposited on the vertically exposed and non-shadowed surfaces. Underneath the undercut its thickness starts to decrease until the n-type poly-Si layer fully disappears before the undercut reaches its maximum lateral depth. On the

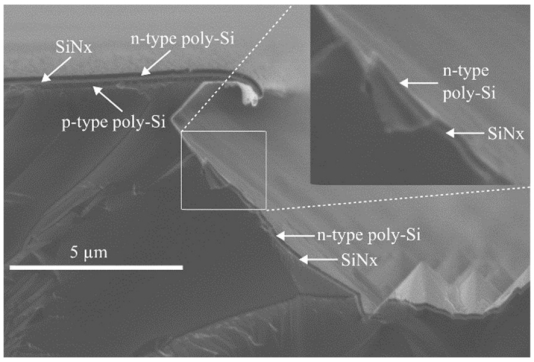


Figure 3: SEM image showing the gap in the n-type poly-Si layer generated by the undercut of the p-type poly-Si at the trench edge. An additional SiN_X dielectric layer, deposited before the n-type poly-Si sputtering enhances the contrast between poly-Si and bulk, but will not be included in a solar cell device.

underside of the undercut we cannot find any n-poly silicon with SEM. With this etched geometry we achieve an approximately 2-3 µm gap between the n-type poly-Si at the bottom of the trench and the n-type poly-Si on top of the p-type poly-Si forming the emitter. Tailoring the etch depth or using isotropic etching allows varying the gap width.

3.3 Proof-of-concept SABC solar cell

Figure 4 a) shows the IV-curve and b) a Lock-In-Thermography (LIT) image of a first SABC cell with an efficiency of 20.2 %. The open circuit voltage V_{OC} yields 708 mV and indicates a reasonable surface passivation, considering that the p-type poly-Si emitter is annealed twice. However, both short circuit current density J_{SC} and fill factor FF are rather low and limit the cell's efficiency. A possible reason for the low J_{SC} could be a process-related low wafer bulk lifetime, which would also affect the FF, which is subject to further analysis and improvement. The series resistance R_S = 0.72 Ωcm² is not the primarily factor limiting the FF with pFF-FF = 3.3 %. The shunt resistance R_{sh} =3.3 kΩcm², extracted from the dark IV-curve, still needs improvement but shows that the gap across the trench edge insulates the two poly-Si layers quite well.

Figure 4 b) shows a thermal map of the cell by Lock-In-Thermography (LIT) under reverse bias. Defects, such as shunts because of incomplete insulation of oppositely doped surfaces, generate heat due to increased current flow. In a typical IBC cell with interdigitated positive and negative contacts, the oppositely doped surfaces come into close contact across most of the back side of the cell and therefore may form shunts. In this cell, the LIT shows mostly local shunts at, or close to, the busbars interconnecting the positive electrodes, while most p-type/n-type poly-Si at the indigitated electrodes appear well insulated. Underneath all busbars interdigital pattern is interrupted and the poly-Si is doped according to the busbar polarity. Two possible causes of shunts at the emitter busbars are currently under investigation: the positive busbars are piercing through the emitter after fast firing of the paste and contact the base, or local shunts across the trench wall only in the busbar area. Given that a non-fire-through paste is used to form the positive busbar, the first option seems unlikely. Instead, we suspect that the laser patterning parameters near the emitter busbar are suboptimal, leading to the formation of shunts across the trench in this region. An improved laser pattern at the emitter busbar should solve these local shunts in the next cell run.

4 CONCLUSIONS

In this contribution, we present the SABC back contact cell concept and show first results on the passivation quality of the p-type poly-Si emitter, the self-aligned insulation and a proof-of-concept solar cell. The solar cell only shows local shunting mostly at the positive busbars contacting the emitter. Across most part of the cell, e.g. between the positive and negative electrodes, the poly-Si layers of opposite polarity are well insulated. Solving the cause of the local shunts and implementing a single annealing step of the emitter should increase the efficiency significantly.

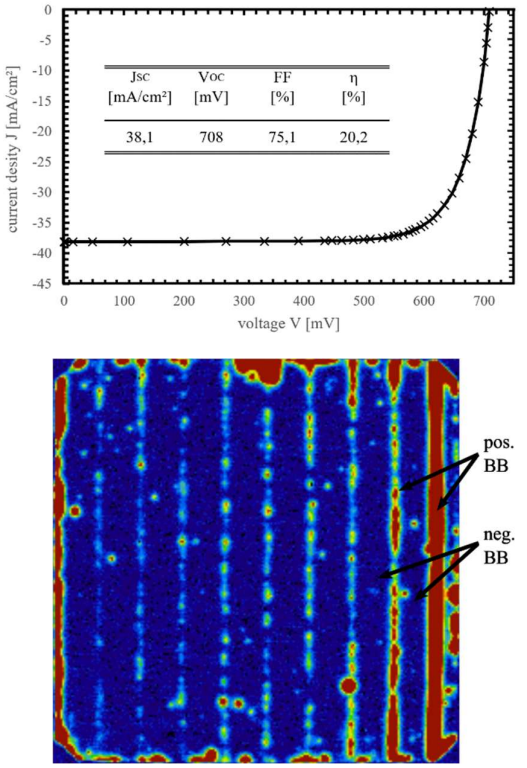


Figure 4: a) IV curve of the best SABC cell so far and b) a lock in thermography image thereof. The cells efficiency is mostly limited by FF and J_{SC} with a V_{OC} = 708 mV showing good surface passivation. The LIT image shows shunts mostly located at the emitter busbars, proving a good insulation between the n-type and p-type poly-Si layer across most of the cell.

5 ACKNOWLEDGEMENTS

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