n-type polysilicon by PVD enabling self-aligned back contact solar cells

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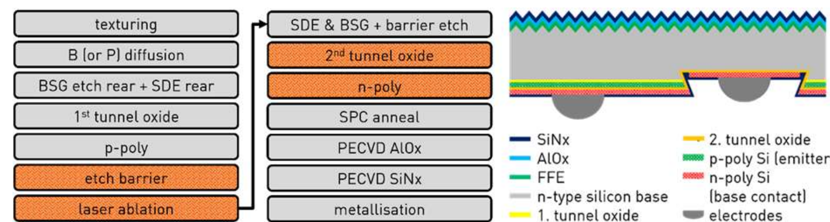
Introduction

- Innovative IBC solar cell process with phosphorous doped *n*-type polysilicon by directional physical vapor deposition (PVD).
- Self aligned separation of the polysilicon contacts via shading from PVD at under-etched trenches.
- Can be integrated into an existing TOPCon manufacturing line with the addition of only two tools
- Investigation of *n*-type polysilicon and *n*-type/*p*-type polysilicon stack on planar and on laser patterned, structured surfaces.

SABC cell design

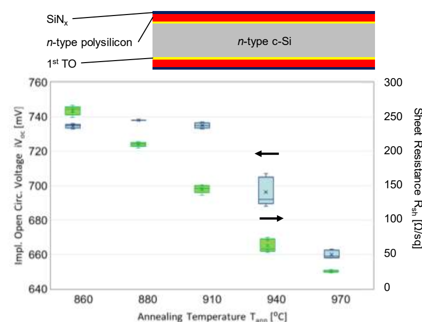


- Additionally required processing steps (orange) compared to TOPCon:
  - etch barrier (EB) deposition
  - laser patterning of EB
  - tunnel oxide (TO) deposition
  - *n*-type polysilicon PVD
- Etching of trenches simultaneous to *p*-poly wrap around etch
- *n*-type polysilicon covers full rear side:
  - except shaded trench edge ⇨ insulation of emitter and base contact
  - n^{++}/p^{++}- tunneling junction at emitter
  - only one metallization step required to contact the *n*-type polysilicon on both passivated contacts

Results

n-type polysilicon:

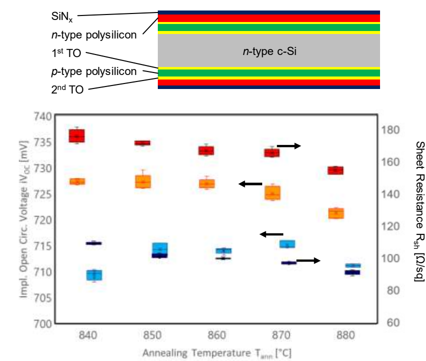
- symmetric TO, n-type polysilicon by PVD on n-type Cz wafers after annealing, passivation with SiN_X and fast firing
- up to iV_{oc} = 738 mV after annealing at T_{ann} = 880 °C
- decreasing sheet resistance R_{sh} with increasing annealing temperature
- for optimum T_{ann} = 880 °C, sheet resistance yields R_{sh} = 208 Ω/sq ⇨ sufficiently low R_{sh} for the base contact of an IBC solar cell



Implied open circuit voltage iV_{OC} and sheet resistance R_{sh} of symmetric *n*-type polysilicon.

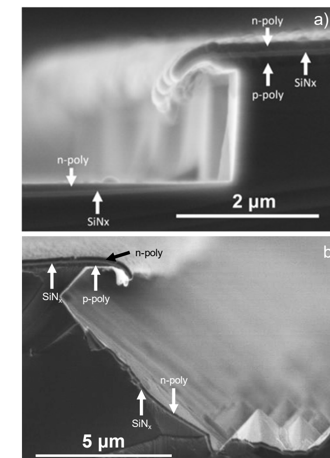
n-type/p-type polysilicon layer stack:

- including 1st and 2nd TO
- symmetric stack on n-type Cz wafer, annealing, SIN_X deposition and fast firing
- up to iV_{OC} = 715 mV after annealing at T_{ann} = 870 °C
- *p*-type polysilicon layer alone yields higher iV_{OC} = 726 mV, indicating lower passivation quality induced by the *n*-type layer
- low sheet resistance R_{sh} = 97 Ω/sq due to the two conductive layers. R_{sh} in good agreement to calculated $R_{sh,ca}$ = 94 Ω/sq from R_{sh} of individual layers



iV_{OC} and R_{sh} of symmetric *p*-type/*n*-type polysilicon including first and second TO.

- SEM image of a trench cross-section after:
  - a) isotropic and b) anisotropic wet-chemical etching of *p*-type polysilicon and c-Si wafer surface
  - etch barrier removal and cleaning
  - SiN_X deposition (to enhance contrast between silicon layers)
  - PVD of *n*-type polysilicon
  - annealing
- Both etchants under-cut barrier layer and *p*-type polysilicon
- *n*-type polysilicon layer thickness (≈ 120 nm) thins as it approaches the trench wall and even disappears
- Separation of *n*-type polysilicon layer across under-cut ⇨ insulation of emitter and base contact



SEM images of a) isotropic and b) anisotropic etched trenches. For both the thickness of the *n*-poly silicon layer reduces as it approaches the trench wall

Conclusion

- High iV_{OC} of base contact *n*-type polysilicon layer and promising iV_{OC} of emitter *n*-type polysilicon/TO/*p*-type polysilicon stack.
- Optimum annealing temperature of both layers in the same range T_{ann} = 870 - 880 °C, hence, enabling co-annealing.
- Low R_{sh} of layer stack indicates low resistance across the interfacial TO between polysilicon layers and allows further optimization of doping concentration and thickness of each layer.
- Wet-chemical etching of *p*-type polysilicon and c-Si wafer surface after laser patterning of SiN_X etch barrier under-cuts both etch barrier and *p*-type polysilicon.
- Under-cut shades subsequent PVD of *n*-type polysilicon at trench edge, hence separating the *n*-type polysilicon layer between base contact and emitter.
- Further proof of contact insulation and first proof of concept solar cells under development.

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